**M.S. Ramaiah Institute of Technology**

**(Autonomous Institute, Affiliated to VTU)**

**Department of CSE**

**CIE II- Scheme and Solutions**

**Course:** Computer Organization **Course Code:** CS1541  **Sem:** IV **Max Marks:** 30

**Instructions to Candidates:** Mobiles, smart watches or any electronic gadgets are strictly banned.

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| **Sl#** | **Question** | **Marks** | **Bloom’s Level** | **CO Mapping** |
| **1** | a) **2.5M**  i) 68 \* -45  -45=1010010  Recoding of -45=110100110  -1 +1 +1 -1  01000100  X -1 +1 +1 -1  11111110111100  000001000100xx  0001000100xxxx  10111100xxxxxx  11010000001100  ii) -25 \* -12 **2.5M**  -12=011001  Recoding of -12= 101000  -1 +1 0  100111  -1 +1 0  11100111XX  011001XXXX  0100101100 | 5 | Apply | CO2 |
| b) Diagram **2M**, explanation including following points **3M**    The datapath for a branch uses the ALU to evaluate the branch condition and a  separate adder to compute the branch target as the sum of the incremented PC and the sign-extended, lower 16 bits of the instruction (the branch displacement), shifted left 2 bits.  The unit labeled *Shift left 2* is simply a routing of the signals between input and output that adds 00two to the low-order end of the sign-extended offset field.  Since we know that the offset was sign-extended from 16 bits, the shift will throw away only “sign bits.” Control logic is used to decide whether the incremented PC or branch target should replace the PC, based on the Zero output of the ALU. | 5 | Understand | CO3 |
| c) Identification of hazard **1M**, solution **4M**  There is a data hazard and can be solved by using data forwarding technique, as shown in the diagram |  |  |  |
|  | 5 | Analyze | CO3 |
| **2** | 1. 52 \* 26 using Carry Save Addition (CSA) technique. 5M   C:\Users\CP\AppData\Local\Microsoft\Windows\Temporary Internet Files\Content.Word\IMG_20160524_110253701.jpg | 5 | Apply | CO2 |
| 1. Abstract view Diagram **2M** explanation **3M**     After the instruction is fetched, the register operands used by an instruction are specified by fields of that instruction.  Once the register operands have been fetched, they can be operated on to compute a memory address (for a load or store), to compute an  arithmetic result (for an integer arithmetic-logical instruction), or a compare (for a branch).  If the instruction is an arithmetic-logical instruction, the result from the ALU must be written to a register.  If the operation is a load or store, the ALU result is used as an address to either store a value from the registers or load a value from  memory into the registers. The result from the ALU or memory is written back into the register file. | 5 | Understand | CO3 |
| 1. Branch prediction method Explanation including example **5M**   Predicting that branches are not taken as a solution to control hazard. The  top drawing shows the pipeline when the branch is not taken. The bottom drawing shows the pipeline when the branch is taken. | 5 | Understand | CO3 |
|  | **OR** |  |  |  |
| **3** | a)  i) 12.125 **2.5M**   |  |  |  | | --- | --- | --- | | 0 | 1000010 | 00..1000010000000.. |   ii) -642.1875 **2.5M**   |  |  |  | | --- | --- | --- | | 1 | 10001000 | 00..01000001010000.. | | 5 | Apply | CO2 |
| b) Each definition 1M  i) Combinational element : An operational element, such as AND or an ALU  ii) State element: A memory element, such as a register or memory.  iii) Clocking methodology: The approach used to determine when data is valid and stable relative to the clock.  iv) Datapath element: A unit used to operate on or hold data within a processor. v) Structural hazard: When a planned instruction can’t execute in the proper clock cycle due to unavailability of hardware. | 5 | Remember | CO3 |
| The pipelined datapath for Instruction decode and Memory access stages for load instruction. Each diagram **2.5M** | 5 | Understand | CO3 |

**Course Outcomes meant to be assessed by the IA Test-II:**

**CO2:** Implement different algorithms used to perform fast multiplication and division also represent the floating-point number in IEEE format.

**CO3:** Design a datapath for MIPS architecture and understand the importance of pipelining.

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